AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method of memory management, comprising:

providing multiple banks of memory devices organized into independent channels wherein each bank of memory devices contains duplicate data;

providing a tree memory controller for controlling data read and write accesses to each of the banks in each of the channels;

establishing a bank queue for each bank in each channel for designating bank availability;

sending read or write requests to the tree memory controller;

checking, at the tree memory controller, the availability of each bank in a channel;

identifying a first available bank; and

executing the read request from the first available bank;

wherein controlling a write access includes blocking all read requests;

confirming that data to be written is complete for the selected memory word length;

waiting for each bank queue to indicate bank availability for all banks;

initiating burst mode transfer of the completed data word to all banks concurrently.

2. (Cancelled)

3. (Original) The method of claim 1 wherein the memory devices comprise dynamic random access memory (DRAM) devices.

4. (Original) The method of claim 1 wherein the memory devices comprise fast cycle random access memory (FCRAM) devices.

5. (Original) The method of claim 1 wherein the banks of memory devices are organized into two independent channels.

6. (Crrently amended) A ~~method~~-system, comprising:

multiple banks of memory devices organized into independent channels wherein each bank of memory devices contains duplicate data;

a tree memory controller for controlling data read and write accesses to each of the banks in each of the channels;

a bank queue for each bank in each channel for designating bank availability; and

means for sending read or write requests to the tree memory controller, said controller determining availability of a bank for reading data and executing the read request from a first available bank;

wherein the controller controls a write access by blocking all read requests, confirming that data to be written is complete for the selected memory word length, waiting for each bank queue to indicate bank availability for all banks, and initiating burst mode transfer of the completed data word to all banks concurrently.

7. (Original) The system of claim 6 wherein the controller suspends all read requests during processing of a write request.

8. (Original) The system of claim 7 wherein the controller writes to all memory banks concurrently.

9. (Original) The system of claim 8 wherein all memory banks contain identical data.

10. (Original) The system of claim 6 wherein the memory banks comprise dynamic random access memory devices.

11. (Original) The system of claim 6 wherein the memory banks comprise fast cycle random access memory devices.

12. (Original) The system of claim 6 wherein the banks of memory devices are arranged in two independent channels.

13. (Original) The system of claim 6 wherein the minimum number of memory banks is determined by the ratio of the random cycle time to the random bank access delay.

14. (New) A method of memory management, comprising:

providing multiple banks of memory devices organized into independent channels wherein each bank of memory devices contains duplicate data;

providing a tree memory controller for controlling data read and write accesses to each of the banks in each of the channels;

establishing a read bank queue and a write bank queue for each bank in each channel for designating bank availability;

sending read or write requests to the tree memory controller;

checking, at the tree memory controller, the availability of each bank in a channel;

identifying a first available bank; and

executing the read request from the first available bank.

15. (New) The method of claim 14, further comprising suspending all read requests during processing of a write request.

16. (New) The method of claim 14 suspending all read requests includes:

blocking all read requests;

confirming that data to be written is complete for the selected memory word length;

waiting for each bank queue to indicate bank availability for all banks;

initiating burst mode transfer of the completed data word to all banks concurrently.

17. (New) The method of claim 14, further comprising writing to all memory banks concurrently.

18. (New) The method of claim 14, wherein the banks of memory devices are arranged in two independent channels.

19. (New) The method of claim 14, wherein a minimum number of memory banks is determined by the ratio of the random cycle time to the random bank access delay.

20. (New) The method of claim 14, wherein the memory devices comprise dynamic random access memory (DRAM) devices

21. (New) The method of claim 14, wherein the memory devices comprise fast cycle random access memory (FCRAM) devices.